CLAIMS

What is claimed is:

1. A method for chemical vapor deposition or atomic layer deposition of aluminum oxide comprising:

(a) providing an aluminum alkoxide precursor that is dissolved, emulsified or suspended in a liquid;

(b) providing a vapor generated from the aluminum alkoxide precursor; and

(c) depositing an aluminum oxide film from said vaporized precursor on a substrate at a temperature greater than 500°C.

2. The method of claim 1 wherein an oxidizing reactant is introduced separately from said vaporized aluminum alkoxide.

3. The method of claim 2 wherein said oxidizing reactant is selected from the group consisting of oxygen, ozone, water, hydrogen peroxide, nitrous oxide, and combinations thereof.

4. The method of claim 1 wherein the aluminum alkoxide precursor includes aluminum alkoxide selected from the group consisting of aluminum iso-propoxide, aluminum sec-butoxide, aluminum ethoxide, aluminum neo-pentoxide, aluminum iso-butoxide, aluminum methoxide, aluminum

propoxide, aluminum butoxide, aluminum tertiary-butoxide, and aluminum phenoxide.

5. The method of claim 1 wherein the liquid is selected from the group consisting of pentane, hexane, octane, heptane, nonane, decane, dodecane, iso-propanol, tetrahydrofuran, and butyl acetate.

6. The method of claim 1 wherein the liquid is selected from the group consisting aliphatic hydrocarbons, aromatic hydrocarbons, alcohols, ethers, aldehydes, ketones, acids, phenols, esters, amines, alkylnitriles, halgonated hydrocarbons, silylated hydrocarbons, thioethers, amines, cyanates, isocyanates, thiocyanates, silicone oils, nitroalkyls, alkylnitrates and/or mixtures of one or more of the above.

7. The method of claim 1 wherein the aluminum alkoxide of said precursor is aluminum iso-propoxide and the liquid is iso-propanol.

8. The method of claim 1 wherein the aluminum alkoxide of said precursor is aluminum iso-propoxide and the liquid is octane.

9. The method of claim 1, wherein the vapor of the aluminum alkoxide precursor is obtained from the vaporization of a mixture of aluminum alkoxide and a liquid wherein the liquid vaporizes at a higher temperature than the aluminum alkoxide such that the liquid is not vaporized when the aluminum alkoxide is

vaporized and the nonvaporized liquid is diverted from the chemical vapor deposition reactor.

10. The method of claim 1 further comprising introducing the vaporized aluminum alkoxide into a reactor with separate addition of an oxidant and an inert purge gas and depositing a film on said substrate by sequential introduction of alternating pulses of vaporized aluminum alkoxide(s), purge gas, co-reactant(s) and purge gas.

11. The method of claim 1 wherein the substrate is selected from the group consisting of semiconductor substrates, dielectrics, metals, organic substrates, glasses, metal oxides, and plastic polymeric substrates, Si-containing semiconductor substrates, silicon on insulator substrates, Si substrates, Ge substrates, SiGe substrates, GaAs substrates, InP substrates and mixtures or multilayers thereof.

12. A multilayer structure incorporating aluminum oxide deposited according to claim 1.

13. A multicomponent film incorporating aluminum oxide deposited according to claim 1.

14. An electronic device that contains aluminum oxide deposited according to claim 1.

15. The electronic device of claim 14 selected from the group consisting of a transistor, capacitor, diode, resistor, switch, light emitting diode, laser, wiring structure, and interconnect.

16. A capacitor structure fabricated by sequentially depositing a bottom electrode layer, a dielectric layer and a top electrode layer on a base structure wherein the dielectric layer incorporates aluminum oxide deposited according to claim 1.

17. The capacitor structure of claim 16 wherein the capacitor structure is selected from the group consisting of stack capacitors and trench capacitors.

18. The capacitor structure of claim 16 further comprising depositing a dielectric buffer layer over the capacitor structure.

19. The capacitor structure of claim 18 wherein the optional dielectric buffer layer is selected from the group consisting of aluminum oxide and a multilayer structure with aluminum oxide and any insulating material wherein aluminum oxide is deposited according to claim 1.

20. The capacitor structure of claim 16 wherein the capacitor structure is connected to underlying circuitry via a plug and optional barrier.

21. The capacitor structure of claim 20 wherein the plug material is selected from the group consisting of polysilicon, W, Mo, Ti, Cr, Cu, and doped or undoped alloys, mixtures or multilayers thereof.

22. The structure of claim 20 wherein the conductive barrier is selected from the group consisting of TaN,

TaSiN, TiAlN, TiSiN, TaSiN, TaWN, TiWN, TaSiN, TaAlN, NbN, ZrN, TaTiN, TiSiN, TiAlN, IrO_2, SiC, TiPt, TiNPt, TiAlN-Pt, Ru, RuO_2, RuPt, RuO_2, WSi, Ti, TiSi, doped and undoped polysilicon, Al, Pd, Ir, IrO_x, Os, OsO_x, MoSi, TiSi, ReO_2, and doped or undoped alloys, mixtures or multilayers thereof.

23. The structure of claim 16 wherein the bottom electrode is selected from the group consisting of conductive materials, polysilicon, Ni, Pd, Pt, Cu, Ag, Au, Ru, Ir, Rh, IrO_x, RuO_x, TaN, TaSiN, Ta, $SrRuO_3$, $LaSrCoO_3$, and doped or undoped alloys, mixtures or multilayers, thereof.

24. The structure of claim 16 wherein the dielectric material is selected from the group consisting of aluminum oxide and a multilayer structure of aluminum oxide and any insulating material.

25. The structure of claim 16 wherein the top electrode is selected from the group consisting of polysilicon, Ni, Pd, Pt, Cu, Ag, Au, Ru, Ir, Rh,IrO_x, RuO_x, TaN, TaSiN, Ta, $SrRuO_3$, $LaSrCoO_3$,and doped or undoped alloys, mixtures or multilayers thereof.

26. A wiring structure formed by etching trenches and vias into a dielectric layer, patterning the metallization layer, depositing an optional barrier material, and depositing a wiring material, wherein the dielectric layer and/or the optional barrier material incorporate aluminum oxide deposited according to claim 1.

27. The structure of claim 26 wherein the dielectric layer is selected from the group consisting of aluminum oxide and multilayers of aluminum oxide and SiO_2, SiO_xN_y, Si_3N_4, phosphosilicate glass, metal oxides, doped or undoped alloys, mixtures or multilayers, thereof, wherein aluminum oxide is deposited according to claim 1.

28. The structure of claim 26 wherein the optional barrier material is selected from the group consisting of aluminum oxide and doped or undoped alloys, mixtures or multilayers, thereof of aluminum oxide and WN, TiN, TaN, SiO_2, SiO_xN_y, Si_3N_4, phosphosilicate glass, metal oxides, wherein aluminum oxide is deposited according to claim 1.

29. The structure of claim 26 wherein the wiring material is selected from the group consisting of polysilicon, Al, W, Mo, Ti, Cr, Cu and doped or undoped alloys, mixtures or multilayers thereof.

30. A structure comprising a substrate having source and drain regions and a channel region between said source and drain regions; depositing a gate dielectric, aligned to and on top of said channel region; and depositing a gate electrode aligned to and on top of said gate dielectric wherein the gate dielectric incorporates aluminum oxide deposited according to claim 1.

31. A method of fabricating an electronic device comprising: providing a silicon substrate having a first region doped with a first dopant type and a second region doped with a second dopant type; forming a gate

dielectric layer on said substrate; forming a mold layer on said gate dielectric; forming a first trench in said mold layer; forming a first liner in said trench, said first liner comprised of an alloy having a first work function; filling said trench with a gate conductor to form a first gate; forming a second trench in said mold layer; forming a second liner in said trench, said first second comprised of an alloy having a second work function; filling said trench with a gate conductor to form a second gate; ion implanting a first dopant type on either side of said second gate to form source drain regions in said substrate; and ion implanting a second dopant type on either side of said first gate to form source drain regions in said substrate wherein the gate dielectric incorporates aluminum oxide deposited according to claim 1.

32. The structure of claim 30 wherein the gate dielectric selected from the group consisting of aluminum oxide and doped or undoped alloys, mixtures or multilayers of aluminum oxide and SiO_2, SiO_xN_y, Si_3N_4, BaO, SrO, CaO, Ta_2O_5, TiO_2, ZrO_2, HfO_2, La_2O_3, Y_2O_3, yttrium alumnate, lathnaum alumnate, lanthanum silicate, yttrium silicate, hafnium silicate, zirconium silicate, wherein aluminum oxide is deposited according to claim 1.

33. The structure of claim 30 wherein the gate dielectric is composed of more than one layer and at least one component of at least one of the layers comprising the gate dielectric is aluminum oxide deposited according to claim 1.

34. The structure of claim 30 wherein the multilayer gate dielectric is composed of a lower, middle and optional upper layer wherein at least one layer or one component of a layer of the gate dielectric is aluminum oxide deposited according to claim 1.

35. The structure of claim 34 wherein the lower layer is selected from the group consisting of SiO_2, SiO_xN_y, Si_3N_4, BaO, SrO, CaO, Ta_2O_5, TiO_2, ZrO_2, HfO_2, Al_2O_3, La_2O_3, Y_2O_3, yttrium alumnate, lathnaum alumnate, lanthanum silicate, yttrium silicate, hafnium silicate, zirconium silicate, and doped or undoped alloys, mixtures or multilayers, thereof.

36. The structure of claim 34 wherein the middle layer is selected from the group consisting of SiO_2, SiO_xN_y, BaO, SrO, CaO, Si_3N_4, Ta_2O_5, TiO_2, ZrO_2, HfO_2, Al_2O_3, La_2O_3, Y_2O_3, yttrium alumnate, lathnaum alumnate, lanthanum silicate, yttrium silicate, hafnium silicate, zirconium silicate, and doped or undoped alloys, mixtures or multilayers, thereof.

37. The structure of claim 34 wherein the upper layer is selected from the group consisting of SiO_2, SiO_xN_y, Si_3N_4, BaO, SrO, CaO, Ta_2O_5, TiO_2, ZrO_2, HfO_2, Al_2O_3, La_2O_3, Y_2O_3, yttrium alumnate, lathnaum alumnate, lanthanum silicate, yttrium silicate, hafnium silicate, zirconium silicate, and doped or undoped alloys, mixtures or multilayers, thereof.

38. The structure of claim 30 wherein the gate electrode is selected from the group consisting of polysilicon, Al,

Ag, Bi, Cd, Fe, Ga, Hf, In, Mn, Nb, Y, Zr, Ni, Pt, Be, Ir, Te, Re, Rh, W, Mo, Cr, Fe, Pd, Au, Rh, Ti, Cr, Cu, and doped or undoped alloys, mixtures or multilayers, thereof.